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Design of Low Power SRAM Array Logic Using Recovery Boosting Technique

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ABSTRACT: Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance at the expense of increased leakage current. Supply voltage scaling is an effective way of reducing dynamic as well as leakage power consumption. However the sensitivity of the circuit parameters increases with reduction of the supply voltage. SRAM bit-cells utilizing minimum sized transistors are susceptible to various random process variations. Hence reducing the memory operating supply voltage, while maintaining the yield is becoming extremely challenging in nano scale technologies. This Paper presents a solution for NBTI in Existing SCHMITT TRIGGER BASED SRAM design by using the Recovery Boosting Technique. This technique is also used in implementing SRAM ARRAY LOGIC with low power. Thus the simulations are carried out in TANNER EDA tools.

KEYWORDS: SRAM, Schmitt Trigger, NBTI, Recovery Boosting Technique, Array Logic.

I. INTRODUCTION

In a given process technology, the maximum supply voltage (referred to as) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits and reducing with the technology scaling due to scaling of the gate-oxide thickness. The minimum SRAM supply voltage, for a given performance requirement (referred to as), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltages [2].
Hence, to enable SRAM bit cell operation across a wide voltage range has to be further lowered. Various design solutions such as read-write assist techniques and bit cell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bit lines, bit cell VSS node, and bit cell VCC node). In order to reduce the considerable in a conventional SRAM cell, Schmitt Trigger based SRAM cell is design which contain 8T [8]. But still this design exhibit Negative Bias Temperature Instability (NBTI) which produces leakage in the design [3]. To overcome the limitations such as NBTI in Existing Design, We proposed simple Recobery Boosting technique. This paper mainly aims at-

- Satisfying the factors like density, volatility, cost and features
- To control the pulse variation and reduce the current leakage in the SRAM circuit
- Reducing the problems arising due to power dissipation and Temperature
- Increasing the efficiency and reliability of SRAM.

II. CONVENTIONAL 6T SRAM CELL

An SRAM cell is the key SRAM component storing binary information [12]. A Typical SRAM cell uses two cross-coupled inverters forming a latch and access transistors. Access transistors enable access to the cell during read and write operations and provide cell isolation during the not-accessed state. An SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention) for as long as the cell is powered. For instance, low-power can compromise the cell area also speed of operation. The mainstream six-transistor (6T) CMOS SRAM cell is four transistors (Q1−Q4) comprise cross-coupled CMOS inverters and two NMOS transistors Q5 and Q6 provide read and write access to the cell. A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation [10].

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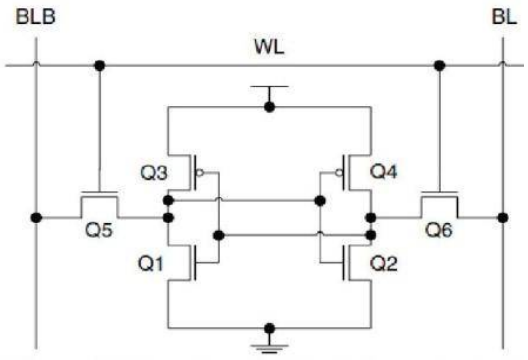

Figure 1: Conventional 6T SRAM Cell

III. EXISTING DESIGN

In order to resolve the conflicting read versus write design requirements in the conventional 6T bit cell, the Schmitt Trigger (ST) principle is applied in the cross-coupled inverter pair [7]. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in figure. During input transition, the feedback transistor (NF) tries to preserve the logic "1" at the output node by raising the source voltage of pull-down NMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics [4]. Since a read-failure is initiated by an input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation [5].

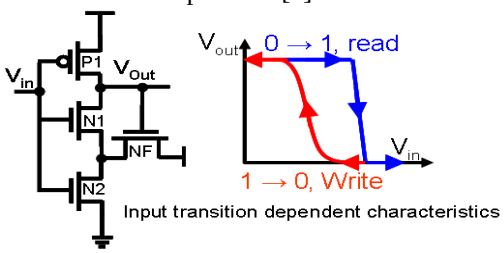

Figure 2**:** Schmitt Trigger Principle

The Existing Circuit is having one transistor (N4) at the bottom of the circuit connected to the ground directly. This particular transistor is having high (Vth) threshold voltage so that the transistor will be switching ON at high voltages . i.e. Whenever voltage fluctuations occur, this transistor will switch ON & dissipate the excess voltage on to the ground. At the same time the transistor at the READ line (N5) is used for separating the read operation without disturbing the write line. When the circuit is with normal input voltages the circuit operates normally providing READ stability, but when the high input voltages are fed, then the excess voltage is dragged by the transistor N4, providing circuit reliability and READ stability through the virtual grounding [6].

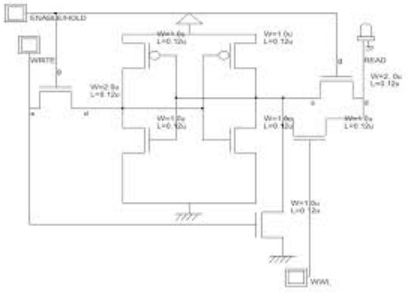

Figure 3: Schmitt Trigger Based SRAM Cell

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During a read operation enable/hold is OFF and N5 becomes ON. The value stored in the cell can read through the transistor N5. Thus separating the read operation from access transistors increases the noise margin of the cell compared to both 6T and ST cells.

III. PROPOSED DESIGN

Negative bias temperature instability (NBTI) has the potential to become one of the main show-stoppers of circuit reliability in nanometer scale devices due to its deleterious effects on transistor threshold voltage [1]. The degradation of PMOS devices due to NBTI leads to reduced temporal performance in digital circuits. We have analyzed the impact of NBTI on the read stability of SRAM cells. We propose a simple solution to reduce the NBTI using a "Recovery boosting" technique.

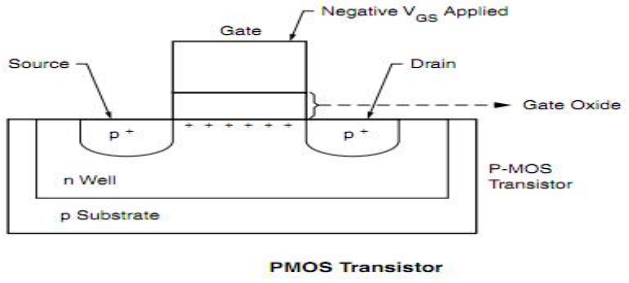

Figure 4: NBTI EFFECT

There are two basic approaches to mitigating NBTI:

- Reduce the stress on the PMOS transistors
- Enhance the recovery process.

Stress reduction techniques aim to reduce the aging rate by controlling and temperature, whereas recovery enhancement techniques aim to increase the recovery time for the PMOS devices. One could implement these techniques at a coarse granularity (e.g., for entire cores) or for individual structures within the core. Recovery boosting is a recovery-enhancement technique for SRAM structures [9]. The following two techniques were most widely used to overcome the above problems

- Stress reduction techniques
- Recovery enhancement techniques

1. RECOVERY BOOSTING TECHNIQUE

We propose a technique called Recovery Boosting that allows both PMOS devices in the memory cell to be put into the recovery mode by slightly modifying to the design of conventional SRAM cells. Previously proposed recovery techniques for SRAM cells aim to balance the degradation of the two PMOS devices by attempting to keep their inputs at a logic "0" exactly 50% of the time.

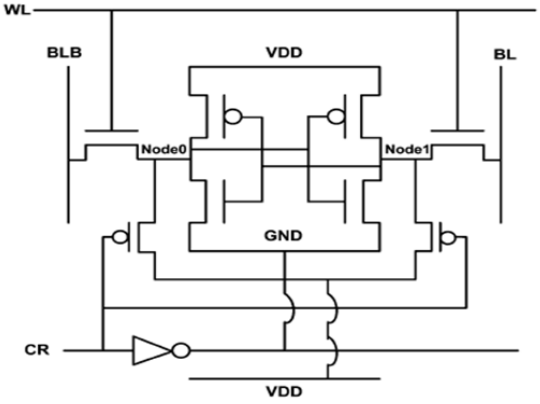

Figure 5: Recovery Boosting Techique

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This can be achieved by raising the ground voltage to the nominal voltage through an external control signal. The modified SRAM cell has the ground connected to the output of an inverter. CR is the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of "1", which in turn connects the ground of the SRAM cell to a value of "0." With this connection, the SRAM cell can perform normal read, write, and hold operations. To apply recovery boosting, CR has to be changed to a "0" in order to raise the ground voltage of the SRAM cell to. This circuit configuration puts both PMOS devices in the SRAM cell into the recovery mode. A cell can be put into the recovery boost mode regardless of whether its wordline (WL) is high or low. Unlike read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its wordline.

MODIFIED SRAM CELL OPERATION

CR	WL	BL	BLB	Node0	Node1	Operation
1	0	X	X	0/1	1/0	Hold
1	1	1	1	0/1	1/0	Read
1	1	1	0	0	1	Write '1'
1	1	0	1	1	0	Write '0'
0	X	X	X	1	1	Recovery Boost

Table 1: SRAM operation

2. ARRAY LOGIC

To provide this isolation, we extend the memory cell with connections to the rail of an adjoining row or column via two pros access devices. Thus an ARRAY LOGIC is built using cascading of proposed design. Thus the power and the effect of NBTI is greatly reduced.

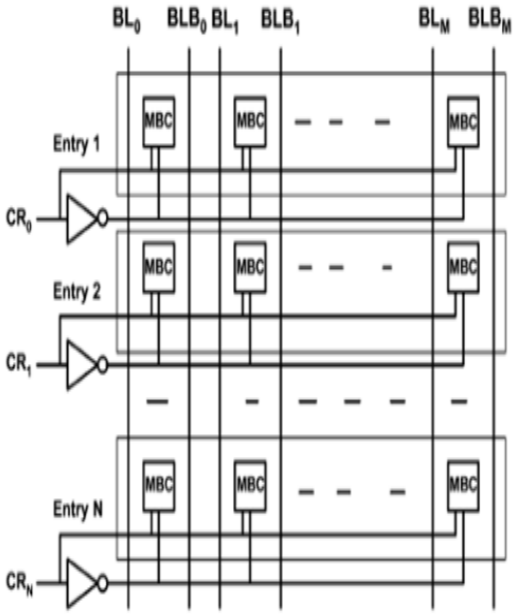

Figure 6: Array Logic

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IV. SIMULATION AND RESULTS

Thus the simulation and the power analysis of proposed designs is as follows,

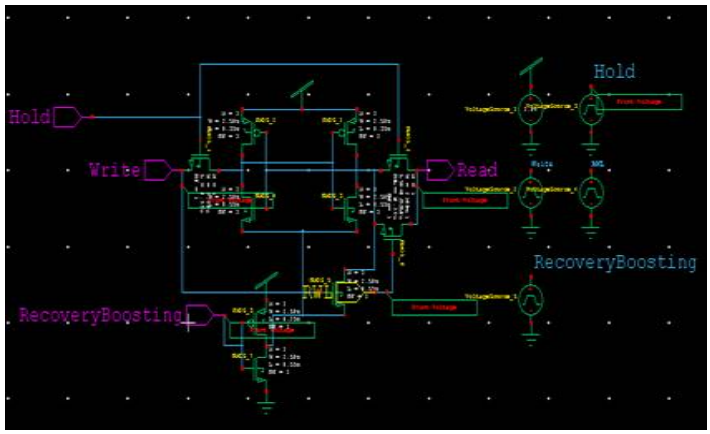

Figure 7: Schematic of SRAM using Recovery Boosting technique

Figure 8: Waveform of SRAM using Recovery Boosting technique

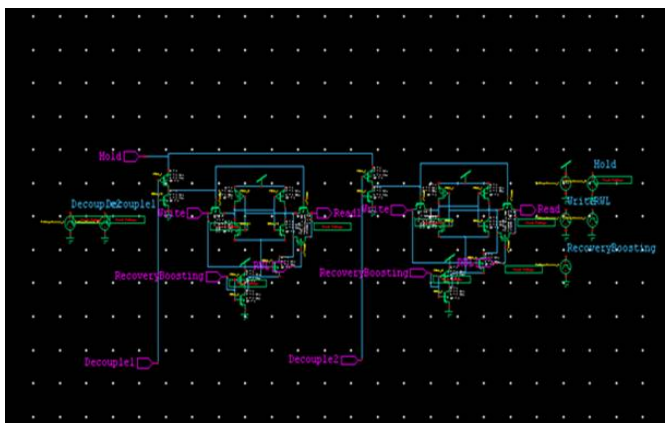

Figure 9: Schematic of Array Logic

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SRAM MODEL	POWER COMSUMPTION
Conventional SRAM	0.25148 mW
Existing Model	1.221 mw
Recovery Boosting	0.09802 mW
SRAM Array model	0.06240 mW

Table 2: Comparison of Power Consumption

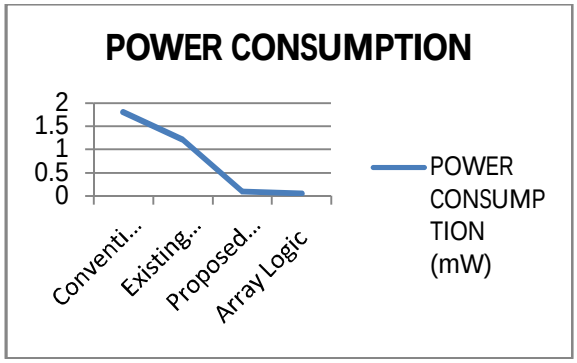

Figure 10: Power Consumption

V. CONCLUSION

In this paper, we presented 6T, Existing Schmitt Trigger (ST) based SRAM cell and Proposed SRAM cell design is analysed for achieving low power consumption. The proposed design shows that much less power compared to conventional 6T SRAM cell and ST based SRAM cells and reduced effects of NBTI. Thus, this design can be used for future SRAM core memories and mobile systems in order to improve the battery efficiency.

REFERENCES

1. M Padmaja, N V Maheswara Rao (2014), "Low Power Design of Schmitt Trigger Based SRAM Cell Using NBTI Technique", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 10, pp. 12664-12670.
2. Ch Harika, Y Sujatha (2014), "High Performance SRAM Design for Low Power Applications", IJSETR, Vol. 3, Issue 45, pp. 9082-9088.
3. Sai Silpa Chandavolu, Prof. K Amarnath (2014, October), "Improved Stability SRAM Design for Low power Applications", International Journal of Application or Innovation in Engineering & Management (IJAIEM), Vol. 3, Issue 10.
4. A Kishore Kumar1, D Somasundareswari, V Duraisamy, T Shunbaga Pradeepa (2014), "Design Of Low Power 8t Sram With Schmitt Trigger Logic", Journal of Engineering Science and Technology, Vol. 9, No. 6, pp. 670 – 677.
5. I Penchala Reddy, Sandeep Kumar Reddy B (2013, july), "Ultralow-Voltage Differential Sensing Schmitt-Trigger-Based SRAM Design", International Journal of Engineering Trends and Technology (IJETT), Vol. 4 Issue 7.
6. Nahid Rahman, B P Singh (2013, March), "Design of Low Power Sram Memory Using 8t Sram Cell", International Journal of Recent Technology and Engineering (IJRTE), Vol. 2, Issue 1.
7. Atluri.Jhansi rani, K Harikishore, Fazal Noor Basha, V G Santhi Swaroop, L. VeeraRaju (2012, May - June), "Designing and Analysis of 8 Bit SRAM Cell with Low Subthreshold Leakage Power", International Journal of Modern Engineering Research (IJMER), Vol.2, Issue.3, pp-733-741.
8. Jaydeep P Kulkarni,and Kaushik Roy (2012, Febrary), "Ultralow-Voltage Process- Variation-Tolerant Schmitt Trigger-Based SRAM Design", IEEE transactions on very large scale integration (vlsi) systems, vol. 20, no. 2.
9. J P Kulkarni, K Kim, S Park, and K Roy (2008, june), "Process variation tolerant SRAM array for ultra low voltage applications", in *Proc. Design Autom. Conf*, pp. 108–113.
10. M M Khellah, A Keshavarzi, D Somasekhar, T Karnik, and V De (2008, June), "Read and write circuit assist techniques for improving of dense 6T SRAM cell", in *Proc. Int. Conf. Integr. Circuit Design Technol.*, pp. 185–189.